CLIPPEDIMAGE= JP402205065A
PAT-NO: JP402205065A
DOCUMENT-IDENTIFIER: JP 02205065 A
TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUBN-DATE: August 14, 1990

INVENTOR-INFORMATION:
NAME
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ASSIGNEE-INFORMATION:
NAME COUNTRY
MATSUSHITA ELECTRON CORP N/A

APPL-NO: JP01024232
APPL-DATE: February 2, 1989

INT-CL_(IPC): H01L027/04; H01L021/90
US-CL-CURRENT: 257/538

ABSTRACT:
PURPOSE: To obtain the resistance of a polycrystalline silicon resistor with high reproducibility by a method wherein a second metal wirings provided on a third insulating film formed on a first metal wiring are directly brought into contact with the surface of the polycrystalline silicon resistor to use the second metal wirings as the integrated circuit internal connection wirings of the polycrystalline silicon resistor.

CONSTITUTION: After a first insulating film 2 is formed on a silicon substrate 1, a polycrystalline silicon resistor 3 doped with P-type impurity is formed. After a second insulating film 4 is formed, a first metal wiring 5 is formed. After a thermal treatment is applied to obtain an ohmic contact with the foundation, a third insulating film 6 is formed by a plasma CVD method. Then organic solvent containing Si is applied to the surface of

the insulating film
6 to form a spin-on-glass layer. After that, a thermal treatment is applied
for leveling, apertures 7 are drilled, second metal wirings 8 are formed and,
after a protective film is formed, a thermal treatment is applied to remove
plasma application damages produced by plasma dry etching.

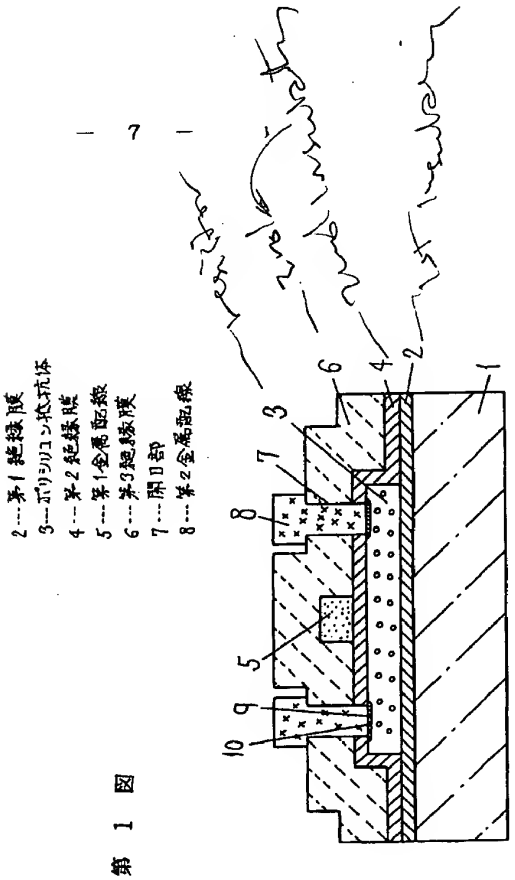
との接触部では第１金属配線のオーミック接触用の熱処理および第３絶縁膜の平坦化熱処理を受けないので、過剰な合金層をおさえ、従って接続部からの合金層のしみ出しを制御でき、ポリシリコン抵抗体の抵抗値のばらつきを低減でき、抵抗値の再現性のよい優れた半導体集積回路装置を実現できる。

4、図面の簡単な説明

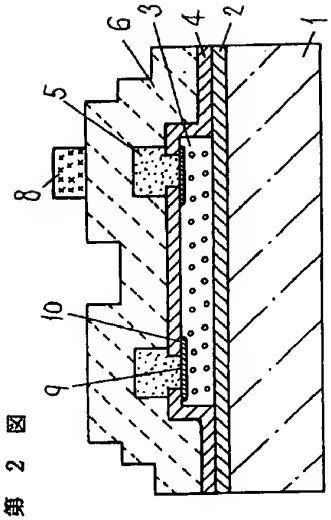
第１図は、本発明の一実施例半導体集積回路装置の断面構造図、第２図は、従来の半導体集積回路装置の断面構造図である。

２……第１絶縁膜、３……ポリシリコン抵抗体４……第２絶縁膜、５……第１金属配線、６……第３絶縁膜、７……開口部、８……第２金属配線。

代理人の氏名　弁理士　栗野重孝　ほか１名



第１図



第２図